ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit device comprises a p-channel MISFET and/or an n-channel MISFET, of which an SRAM cell is constituted and which is arranged to have an offset structure, and MISFET for selection of SRAM cells and MISFET constituting a peripheral circuit of SRAM or a logic circuit which is arranged to have a non-offset structure. At least one of MISFET's constituting an SRAM cell is arranged to take a measure against GIDL (gate induced drain leakage) current.